AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-6 (Canceled).

Claim 7 (Currently amended): A serial/deserializer transmission system, comprising:

a plurality of demodulators, each of the plurality of demodulators receiving signals from one of a plurality of transmission bands that are transmitted on a single electrically differential conductive pair, at least one of the plurality of demodulators comprising:

an analog down converter that converts an input signal from the one of the plurality of transmission bands to a base band;

a filter coupled to receive signals from the down converter, the filter substantially filtering out signals not in the base band;

an analog-to-digital converter coupled to receive signals from the filter and generate digitized signals;

an equalizer coupled to receive the digitized signals; and

a decoder coupled to receive signals from the equalizer and generate recreated data, the recreated data being substantially the same data transmitted by a corresponding modulator,

wherein the plurality of demodulators recover a plurality of bits synchronously distributed across the plurality of transmission bands in the serial/deserializer transmission system, the plurality of demodulators being synchronous to each other.

Claim 8 (Previously presented): The system of Claim 7, wherein the analog down-converter creates an in-phase signal and a quadrature signal, the in-phase signal being the input signal multiplied by a cosine function at the frequency of the one of the plurality of transmission bands and the quadrature signal being the input signal multiplied by a sine function at the frequency of the one of the plurality of transmission bands corresponding to that one of the plurality of demodulators.

Claim 9 (Original): The system of Claim 8, wherein the filter includes an in-phase filter filtering the in-phase signal and a quadrature filter filtering the quadrature signal.

Claim 10 (Original): The system of Claim 9, further including an offset block coupled between the down-converter and the filter, the offset block offsetting the in-phase signal and the quadrature signal such that signals output from the analog-to-digital converter averages zero.

Claim 11 (Original): The system of Claim 8, further including an amplifier coupled between the filter and the analog-to-digital converter, the amplifier amplifying an in-phase filtered signal from the in-phase filter and a quadrature filter signal from the quadrature filter such that the analog-to-digital converter is filled.

Claim 12 (Original): The system of Claim 11, wherein an in-phase gain of the amplifier and the quadrature gain of the amplifier are adaptively chosen in an automatic gain controller.

Claim 13 (Original): The system of Claim 12, wherein the automatic gain controller sets the in-phase gain and the quadrature gain based on the digitized signals from the analog to digital converters.

Claim 14 (Original): The system of Claim 13, wherein the in-phase gain and the quadrature gain are equal.

Claim 15 (Original): The system of Claim 8, wherein the analog-to-digital converter includes a first analog-to-digital converter coupled to receive signals from the in-phase filter and a second analog-to-digital converter coupled to receive signals from the quadrature filter.

Claim 16 (Original): The system of Claim 15, further including a correction circuit coupled between the analog-to-digital converter and the equalizer.

Claim 17 (Original): The system of Claim 16, wherein the correction circuit includes an adjustment to correct phases between the in-phase signal and the quadrature signal.

Claim 18 (Original): The system of Claim 17, wherein a small portion of one of the in-phase signal and the quadrature signal are added to the opposite one of the in-phase signal and the quadrature signal.

Claim 19 (Original): The system of Claim 18, wherein a second portion of the opposite one of the in-phase signal and the quadrature signal is added to the opposite one of the in-phase signal and the quadrature signal.

Claim 20 (Original): The system of Claim 19, wherein the small portion and the second portion are adaptively chosen.

Claim 21 (Original): The system of Claim 20, wherein the small portion is a function of in-phase and quadrature output signals from the correction circuit.

Claim 22 (Original): The system of Claim 20, wherein the second portion is a function of the ratio between in-phase and quadrature signals from the correction circuit.

Claim 23 (Original): The system of Claim 8, wherein a phase rotator circuit is coupled between the analog-to-digital converter and the equalizer.

Claim 24 (Original): The system of Claim 23, wherein a parameter of the phase rotator circuit is adaptively chosen.

Claim 25 (Previously presented): The system of Claim 8, wherein an amplifier is coupled between the equalizer and the decoder.

Claim 26 (Previously presented): The system of Claim 25, wherein a quadrature correction is coupled between the amplifier and the decoder.

Claim 27 (Previously presented): The system of Claim 26, wherein an offset circuit is coupled between the quadrature correction and the decoder.

Claim 28 (Original): The system of Claim 25, wherein an in-phase gain and a quadrature gain of the amplifier are adaptively chosen from error signals calculated from sliced values.

Claim 29 (Previously presented): The system of Claim 28, wherein the sliced values are determined from input signals to the decoder.

Claim 30 (Original): The system of Claim 26, wherein a parameter of the quadrature correction is adaptively chosen.

Claim 31 (Original): The system of Claim 27, wherein a parameter of the offset circuit is adaptively chosen.

Claim 32 (Original): The system of Claim 7, wherein the equalizer is a complex equalizer executing a transfer function, the transfer function having parameters $C_k^x(j)$ and $C_k^y(j)$ where j is an integer.

Claim 33 (Original): The system of Claim 32, wherein the center parameters $C_k^x(0)$ and $C_k^y(0)$ are fixed.

Claim 34 (Original): The system of Claim 33, wherein $C_k^x(0)$ is one and $C_k^y(0)$ is zero.

Claim 35 (Original): The system of Claim 33, wherein the parameters $C_k^x(-1)$ and $C_k^y(-1)$ are fixed.

Claim 36 (Original): The system of Claim 35, wherein the parameter $C_k^x(-1)$ is about -0.3125.

Claim 37 (Original): The system of Claim 35, wherein the parameter $C_k^y(-1)$ is about -0.015625.

Claim 38 (Currently amended): A method of receiving data in a serial/deserializer system, comprising:

receiving an input signal into a plurality of demodulators coupled to a single conducting differential pair, each of the plurality of demodulators receiving signals from one of a plurality of transmission bands <u>synchronously with others of the plurality of demodulators</u>, a plurality of bits

having been synchronously encoded and transmitted across the plurality of transmission bands, each of the plurality of demodulators including

analog down-converting the input signal to obtain a base band signal corresponding to that one of the plurality of transmission bands;

filtering the base band signal to remove signals not in the base band;

digitizing the filtered base band signal to obtain a digitized signal;

equalizing the digitized signal; and

decoding the digitized signal to recover data that is substantially the same as that transmitted by a corresponding modulator in a transmitter,

wherein the plurality of bits synchronously transmitted across the plurality of transmission bands of the serial/deserializer system is recovered.

Claim 39 (Previously presented): The method of claim 38, wherein down-converting the input signal includes:

multiplying the input signal by a cosine function at the frequency of the one of the plurality of transmission bands to obtain an in-phase signal; and

multiplying the input signal by a sine function at the frequency of the one of the plurality of transmission bands to obtain a quadrature signal,

wherein the base band signal includes the in-phase signal and the quadrature signal.

Claim 40 (Previously presented): The method of claim 38, further including:

offsetting the base band signal so that the averaged digitized signal is zero; and

amplifying the base band signal so that a full range of digitized signal is obtained.

Claim 41 (Previously presented): The method of claim 39, further including adjusting the phase between the in-phase signal and the quadrature signal of the base band signal.

Claim 42 (Previously presented): The method of claim 39, further including providing a quadrature correction.

Claim 43 (Previously presented): The method of claim 39, further including slicing recovered data.

Claim 44 (Previously presented): The method of claim 38, further including adaptively choosing at least one operating parameter.

Claim 45 (Currently amended): A receiver system in a serial/deserializer system, comprising:

means for receiving an input signal from a single conductive differential pair, the input signal including a plurality of transmission bands; and

for each of the plurality of transmission bands,

means for down-converting the input signal to receive a base-band signal;

means for obtaining a digital signal from the base-band signal;

means for equalizing the digital signal; and

means for decoding the digital signal to recover data transmitted by a corresponding modulator in a transmitter coupled to the single conductive differential pair,

wherein a plurality of bits that were synchronously transmitted across the plurality of transmission bands is recovered, and the means for down-converting, means for obtaining, means for equalizing, and means for decoding for each of the plurality of transmission bands are synchronous to each other.